

New FPGAs slot into heterogeneous DSP systems



By John Wemekamp



There is no doubt that FPGAs with their large arrays of multipliers have transformed the repetitive, parallel processing of sensor data at the front end of DSP systems such as radar, signals intelligence, and Electro-Optical/Infrared (EO/IR). Although earlier FPGAs offered the computational performance required, integrating the FPGA with the next level of processing while achieving optimal performance and dataflows required specialized skills as well as intimate application knowledge. The latest generation of FPGAs incorporates a much greater complement of high-speed serial I/O and embedded hard cores and/or vendor-supplied standard interface blocks such as PCI Express and Serial RapidIO. This makes them ideal for use within heterogeneous (mixed FPGA and processor) multicomputing systems. For maximum usability, this extra functionality must be supported by IP libraries and communications middleware to provide a flexible, high-performance dataflow architecture without the integration headaches.

Most military embedded computing applications have severe space, weight, and power constraints motivating designers to consider innovative remedies using the remarkable functionality of today's FPGA devices to achieve true System-on-Chip (SoC) solutions. However, complex sensor processing applications with many hundreds of channels and high data rates are unlikely to be resolved by FPGAs alone. While they are ideally suited to repetitive fixed-point algorithms such as convolution, filtering, and decimation, the resultant data streams will often need to be distributed to a further level of processing. In a large system, this would be an array of multicore Power Architecture processors with AltiVec vector processing enhancements. Such a mixed architecture is also better at supporting complex but variable processing solutions typically found in multimode radars, where an FPGA's reconfigurability can be exploited to optimize a radar's performance in different modes of operation.

Serial connectivity

In common with other embedded sectors, there has been a rapid migration of standards-based connectivity from parallel standards such as PCI and PCI-X to the serial connectivity of PCI Express, Serial RapidIO, and Ethernet. In the military embedded market, this has been facilitated by the introduction of the VPX (VITA 46) standard and the widespread use of Freescale Semiconductor's 8641D dual core Power Architecture processor, creating a new fabric-based framework for the implementation of complex multicore node solutions. Through advances in process technology, the latest FPGA devices – such as Xilinx's Virtex-5 or Altera's Stratix IV – incorporate many more multipliers and logic elements. They also include a significant step forward in multi GHz, high-speed I/O signaling to satisfy the new serial fabric and networked vision of system connectivity. For example, the Virtex-5 includes up to four scalable PCI Express endpoints, configurable from x1 to x8 lanes, and Serial RapidIO soft cores, as well as up to eight 10/100/1000 Mbps Ethernet Media Access Controllers (MACs).

Military DSP solutions require advanced Direct Memory Access (DMA) controllers and banks of external memory (SRAM and DDR2 DRAM) to support the buffer sizes, dataflows, and fabric ports needed to process incoming streams of data produced by Synthetic Aperture Radar (SAR) or electronics intelligence gathering equipment. In the case of the multimode radar mentioned earlier, these dataflows may vary between modes in their bandwidth and routing, highlighting the need for the flexibility offered using a switched fabric compared to fixed, point-to-point links. But the key to making use of all this additional capability lies in a common interprocessor communications layer between all processing nodes within a system, whether FPGA or Power Architecture, and a set of IP cores and tools to ease their integration.

Together with the serial standards connectivity framework, these tools and IP make it possible to implement more efficient DSP solutions with mixed processing technologies, focusing on algorithm development, distribution of tasks, and dataflow rather than the time-consuming integration of disparate technologies. These principles are illustrated by the CHAMP-FX2 from Curtiss-Wright Controls Embedded Computing (CWCEC) shown in Figure 1. The VPX-compatible CHAMP-FX2 incorporates two Virtex-5 devices and a dual core 8641D processor, supported by Continuum FXtools. It includes IP in support of Serial RapidIO DMA engines, external memory controllers, and a scalable switching interconnect. All these are optimized for operation over rugged temperature ranges.



Figure 1

Today, many more mixed sensor/general-purpose processing applications are turning to FPGAs for an affordable, practical solution. Practical heterogeneous computing architectures will be the way to resolve the diminishing space, weight, and power versus performance dilemma. FPGA devices properly supported by COTS vendors' IP and tools, such as the Virtex-5 or Stratix IV, have the logical, arithmetic, and I/O capability to perform front-end DSP operations. In addition, they can slot into heterogeneous, serial-standards based computing systems, satisfying the military's complex future multicomputing applications.

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