

## **Curtiss-Wright's New Inter-Processor Communications (IPC) Software Supports SRIO, Switched Serial Fabric on VPX Boards**

*Software Library Simplifies Development of Switched Interconnect Solutions with Messaging and Global Shared Memory Support*

LEESBURG, VA – December 21, 2006, -- Curtiss-Wright Controls Embedded Computing has introduced IPC 2.0, the latest version of its popular Inter-Processor Communications (IPC) software library for building high-performance multi-processor DSP VPX and VPX/REDI-based (VITA 46/VITA 48) platforms employing switched interconnect technology. IPC 2.0 is designed for use in demanding signal processing applications such as radar, sonar and signal intelligence. The new IPC 2.0, with its support for Serial RapidIO (SRIO), makes Curtiss-Wright's DSP communications library ideal for DSP applications designed with the latest high bandwidth, switched serial fabric-based VPX technology.

"IPC 2.0 delivers on our investment in abstracting the hardware layers of our new VPX DSP boards to ease migration between product generations," said Lynn Patterson, vice president and general manager of Modular Solutions, Curtiss-Wright Controls Embedded Computing. "Because IPC 2.0 is completely interoperable with earlier versions of IPC, which supported PCI and StarFabric, it greatly eases customer migration from legacy DSP engines from Curtiss-Wright into the new switched serial fabric architectures. As the cornerstone of our multi-processor software strategy, our IPC library software greatly simplifies and speeds the development of our customer's switched interconnect solutions."

IPC 2.0 supports two communications models. Its messaging API provides the foundation for control and synchronization between processors with priority-based, flow-controlled and acknowledged messages. IPC 2.0 also provides a global shared memory model that is used for the transfer of large datasets. With support for global shared memory, IPC 2.0 eases the porting of software between Curtiss-Wright hardware and middleware environments from other DSP engine vendors, making it faster and simpler to migrate from legacy VME64x-based platforms to the new high performance VPX/VPX-REDI architectures.

IPC 2.0 supports Curtiss-Wright's new VPX and VPX-REDI cards, including the single and dual-core versions of the CHAMP-AV6 DSP engine and the single and dual-core versions of the VPX6-185 single board computer (SBC). IPC 2.0 is designed to extract maximum performance from the SBC's underlying hardware and automatically makes use of technologies on the boards, such as the CHAMP-AV6's SRIO messaging unit and Freescale 8641 DMA controllers.

### **IPC 2.0 VPX/VPX-REDI Hardware Support:**

- CHAMP-AV6 Quad PowerPC 8641/8641D DSP engine
- SVM/DMV-185 PowerPC 8641/8641D SBC

The IPC library also provides support for high availability systems. With functionality to allow dynamic entry and exit of nodes from a system, developers can construct systems with n+1 redundant sparing techniques that exhibit minimal downtime to reconfigure after a board failure.

### **IPC 2.0 Functionality**

IPC 2.0 provides prioritized, queue-driven flow-controlled message passing for command and control as well as block transfers for high-volume time-perishable data. A POSIX compliant interface is provided with standard *open*, *close*, *read*, *write*, and *ioctl* functions. An extended interface provides control over additional features.

IPC 2.0 also provides a single API for task-to-task communications where tasks can be resident on the same processor, same board, or on boards connected via switched interconnect. The unified API greatly eases the design of building scalable software, as senders and receivers can be moved around the system without source code changes, or redesign of routing control. The hardware abstraction provided by IPC 2.0, means that software developed using IPC 2.0 will port easily to future architectures and alternative switched interconnect technology.

Data transport features in IPC 2.0 address common scenarios in signal processing algorithms where frequently, a single data matrix is divided between processors and reconstructed during the processing stages. For corner turn operations, IPC supports multiple senders writing to a single receiver and strided data movements to facilitate operation on large matrices that have been partitioned. When supported by the operating system, IPC 2.0 can perform copyless message retrieval to eliminate the time wasted by making local copies of incoming messages.

IPC 2.0 is supported for use with the VxWorks 6.3 real-time operating system from Wind River.

Availability of IPC 2.0 is immediate. The IPC library is included with the board support package for single card applications.

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### **About Curtiss-Wright Controls Embedded Computing**

Curtiss-Wright Controls Embedded Computing is the industry's most comprehensive and experienced single source for embedded solutions, ranging from Processing, Subsystems, Data Communication, DSP, and Video & Graphics to the most advanced board level components and fully integrated custom systems. The Embedded Computing group serves the defense, aerospace, commercial and industrial markets and is part of Curtiss-Wright Controls Inc. For more information about Curtiss-Wright visit [www.cwcembedded.com](http://www.cwcembedded.com).

### **About Curtiss-Wright Controls, Inc.**

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